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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/016,939

12/14/2001

Glen E. Roeters

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10/19/2005

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EXAMINER

ZARNEKE, DAVID A

ART UNIT

PAPER NUMBER

2891

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/016,939

Applicant(s)

ROETERS ET AL.

Examiner

David A. Zarneke

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 10-21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 8/9/05 have been fully considered but they are not persuasive. Four arguments were presented and are addressed below.

The first argument is that the rejection does not address a flex circuit. It only addresses a flex substrate.

The examiner notes that the claims require a flex circuit comprising a flex substrate; a conductive pattern; a plurality of leads; and at least two IC chips connected to the pattern. Therefore, the rejection's assertion that Watanabe teaches each of these elements means that a flex circuit is taught by Watanabe.

The second argument presented is that the examiner's assertion that the base plate of Watanabe meets the claims requirement that the substrate (and circuit) be flexible is contrary to the plain meaning of the word flexible.

It is the examiner's position that the metes and bounds of the word flexible is not defined in the specification, therefore the word is given its broadest reasonable meaning. The examiner asserts all substrates are flexible, under the proper conditions. Any substrate can be made to bend. Therefore, the flexible limitation has been met by Watanabe.

The third argument presented is that Watanabe teaches unpackaged dies while the claims require packages.

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The examiner asserts that Watanabe only teaches that the dice are not SEALED in a package. Especially in light of Figures 3, 5, 9, 10, 12, 16, and 17, which clearly teach packaged dice. These figures teach dice packaged in a molding [7] and attached to wirings [5] (figures 3, 5, 9, 10 & 12) or even attached to a plastic film tape [103] (figures 16 & 17).

The final argument presented is that Watanabe fails to teach a CSP package (claim 8) and/or a BGA package (claim 9).

As noted in the previous office action and here again, the examiner points out that Watanabe fails to teach these types of packages. The rejection goes on to say that one of ordinary skill in the art would use these types of packages in Watanabe because they are conventional package types equivalent to the ones of Watanabe. Especially given the various types of packages Watanabe teaches in Figures 3, 5, 9, 10, 12, 16, and 17.

Therefore the previous office action is maintained and is repeated below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe et al., US Patent 4,982,265.

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Watanabe (figures 1 & 2) teaches a chip stack comprising:

a flex circuit comprising;

a flex substrate [1];

a first conductive pattern (5, 66+) disposed on the flex substrate; and a plurality of leads [2] extending from the flex substrate and electrically connected to the first conductive pattern (5, 66+);

at least two integrated circuit chip packages [4A-D] electrically connected to the first conductive pattern.

Watanabe teaches that the flex substrate is made of a ceramic (5, 38+), which is flexible to at least some degree. The specification does not define what flexible means. There is no quantification for the term flexible, therefore a ceramic material meets the limitation of the claims because all things are flexible, at least to some degree.

Regarding claim 2, Watanabe teaches the flex substrate defines opposed top and bottom surfaces; and

the first conductive pattern comprises:

a first set of flex pads disposed on the top surface of the flex substrate (5, 66+); and

a second set of flex pads disposed on the bottom surface of the flex substrate (6, 15+);

the flex pads of the first and second sets being electrically connected to the leads (5, 66+ & 6, 15+), with one of the integrated circuit chip packages being disposed upon the top surface of the flex substrate and electrically connected to at least

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some of the flex pads of the first set and one of the integrated circuit chips being disposed upon the bottom surface of the flex substrate and electrically connected to at least some of the flex pads of the second set (figure 2).

With respect to claim 3, Watanabe teaches the flex pads of the first and second sets are arranged in identical patterns (figure 2).

As to claim 4, Watanabe teaches the flex substrate has a generally rectangular configuration defining opposed pairs of longitudinal and lateral peripheral edge segments; and the leads extend from at least one of the longitudinal and lateral peripheral edge segments of the flex substrate (figures 1 and 2).

Regarding claim 6, Watanabe teaches the integrated circuit chip packages each comprise:

- a package body [4A-D] having opposed, generally planar top and bottom surfaces; and

- a plurality of conductive contacts disposed on the bottom surface of the package body (5, 49+);

the conductive contacts of one of the integrated circuit chip packages being electrically connected to respective ones of the flex pads of the first set, with the conductive contacts of one of the integrated circuit chip packages being electrically connected to respective ones of the flex pads of the second set (figure 2).

With respect to claim 7, Watanabe teaches the flex pads of the first and second sets and the conductive contacts are arranged in identical patterns (figure 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 5, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al., US Patent 4,982,265, as applied to claim 1 above.

In re claim 5, though Watanabe fails to teach each of the leads is an S-lead, barring a showing of unexpected results, it would have been obvious to one of ordinary skill in the art to use S-leads in place of the leads of Watanabe because the lead type is interchangeable and S-leads would allow attached to another substrate without having to form openings in the other substrate.

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

As to claim 8, though Watanabe fails to teach each of the integrated circuit chip packages comprises a CSP device, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a CSP device as the chip of Watanabe because CSP devices are commonly used in the art chips. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

In re claim 9, though Watanabe fails to teach the integrated circuit chip packages are each selected from the group consisting of: a BGA device; a fine pitch BGA device; and a flip chip device, barring a showing of unexpected results it would have been obvious to one of ordinary skill in the art at the time of the invention to use a BGA device; a fine pitch BGA device; or a flip chip device as the chip of Watanabe because these are commonly used equivalents chip packages used in the art.

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The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Conclusion

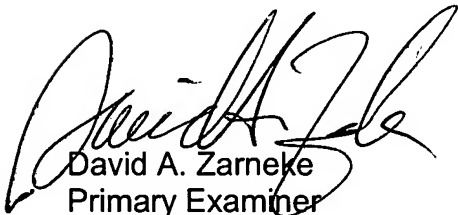
THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication from the examiner should be directed to David A. Zarneke at (571)-272-1937. The examiner can normally be reached on M-F 7:30 AM-6 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1722. The fax phone number for the organization where this application is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read "David A. Zarneke", is written over the printed name and title.

David A. Zarneke
Primary Examiner
October 15, 2005